IN THE CLAIMS:

Please amend the claims as follows:

1(original). A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer formed on the first surface, onto a base material on which a predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to said base material;

removing a predetermined amount of said metal layer to form an opening having a first diameter at a position where a connection with said wiring pattern is to be attained;

irradiating a laser beam toward said resin layer through said resin removed region to form a blind via hole having a diameter smaller than that of said opening, so that said wiring pattern is exposed at a bottom of said blind via hole and a step portion of the resin substrate remains adjacent a periphery of said blind via hole;

A1

electroless plating to form an electroless plated film on said exposed wiring pattern, a side wall of said blind via hole, the step portion of said exposed resin layer, and at least a portion of the metal layer adjacent a periphery of said opening;

electro plating at a density of electric current of 0.1 to 2 A/dm^2 to form an electro plated film on said electroless plated film so that a plating deposition speed on a face of an electroless plated film in said blind via hole is higher than that on a substantially flat surface of electroless plated film on said metal layer formed on the resin layer; and

after said electro plating, etching said metal layer to form a predetermined wiring pattern.

2(original). A process as set forth in claim 1, wherein the first diameter of said opening of the metal layer is smaller than a second diameter of the wiring pattern.

3(original). A process as set forth in claim 1, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

4(original). The process of claim 1 wherein the periphery of the blind via hole has a diameter of from about 20 to 100 μm, and wherein the plating current density is 0.5 to 1.5 A/dm^2.

5(original). The process of claim 1 wherein the plating current density is about 1 A/dm^2, and the thickness of the electroless plated film is between about 0.5 to about 3.0 μm.

6(original). A process for producing a multilayer wiring board comprising the following steps of:

forming a resin layer onto an electrically insulating base material on which a predetermined wiring pattern is formed;

adhering a metal layer onto said resin layer;

removing a predetermined amount of said metal layer to form an opening having a first diameter at a position where a connection with said wiring pattern is to be attained;

irradiating a laser beam toward said resin layer through said resin removed region to form a blind via hole having a diameter smaller than that of said opening, so that said wiring pattern is exposed at a bottom of said blind via hole and a step portion of the resin substrate remains adjacent a periphery of said blind via hole;

electroless plating to form an electroless plated film on said exposed wiring pattern, a side wall of said blind via hole, the step portion of said exposed resin layer, and at least a portion of the metal layer adjacent a periphery of said opening;

electro plating at a density of electric current of 0.1 to 2 A/dm^2 to form an electro plated film on said electroless plated film so that a plating deposition speed on a face of an electroless plated film in said blind via hole is higher than that on a substantially flat surface of electroless plated film on said metal layer formed on the resin layer; and

after said electro plating, etching said metal layer to form a predetermined wiring pattern.

7(original). A process as set forth in claim 6, wherein the first diameter of said opening of the metal layer is smaller than a second diameter of the wiring pattern.

A1

8(original). A process as set forth in claim 6, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

9(original). The process of claim 6 wherein the periphery of the blind via hole has a diameter of from about 20 to 100 μm, and wherein the plating current density is 0.5 to 1.5 A/dm^2.

10(original). The process of claim 6 wherein the plating current density is about 1 A/dm^2, and the thickness of the electroless plated film is between about 0.5 to about 3.0 μm.

11(original). A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate onto a base material on which a predetermined wiring pattern is formed, so that a surface of the resin substrate covers said wiring pattern;

irradiating a laser beam toward said resin layer to form a blind via hole having a diameter r of from about 20 to 100 μm and a depth h of from about 20 to 100 μm wherein the ratio h/r is from about 0.5 to 1.5, so that said wiring pattern is exposed at a bottom of said blind via hole;

electroless plating to form an electroless plated film on said exposed wiring pattern and a side wall of said blind via hole;

forming a resist on electroless plated film except for the region of said via hole and the periphery thereof;

electro plating at a density of electric current of 0.1 to 2 A/dm^2 to form an electro plated film on said electroless plated film except for said resist so that a plating deposition speed on a face of an electroless plated film in said blind via hole is higher than that on a substantially flat surface of electroless plated film on said metal layer formed on the resin layer; and

A1

removing said resist and subsequently said electroless plated film under said resist, so that said blind via hole is filled with said electro plated film.

12(original). A process as set forth in claim 11, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

13(original). The process of claim 11 wherein the periphery of the blind via hole has a diameter of from about 20 to 50 μm, and wherein the plating current density is 0.5 to 1.5 A/dm^2.

14(amended). A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer ~~is~~ formed on the first surface, onto a base material on which a first predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to said base material;

removing a portion of said metal layer to expose a portion of the resin layer;

irradiating a laser beam toward said resin layer to form a blind via hole having a diameter r of from about 20 to 100 μm and a depth h of from about 20 to 100 μm wherein the ratio h/r is from about 0.5 to 1.5, so that a portion of said wiring pattern is exposed at a bottom of said blind via hole;

electroless plating to form an electroless plated film on said exposed wiring pattern and a side wall of said blind via hole;

~~forming a resist on electroless plated film except for the region of said exposed wiring pattern, a side wall of said blind via hole, and the step portion of said exposed resin layer;~~

electro plating at a density of electric current of 0.1 to 2 A/dm^2 to form an electro plated film on said electroless plated film ~~except for said resist~~ so that a plating deposition speed on a face of an electroless plated film in said blind via hole is higher than that on a substantially flat surface of electroless plated film on said metal layer formed on the resin layer; and

~~removing said resist and subsequently said electroless plated film under said resist, so that said blind via hole is substantially filled with said electro plated film~~ etching said metal layer to form a second predetermined wiring pattern.

15(original). A process as set forth in claim 14, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

16(original). The process of claim 14 wherein the periphery of the blind via hole has a diameter of from about 20 to 100 μm.

17(original). The process of claim 14 wherein the periphery of the blind via hole has a diameter of from about 20 to 50 μm, and wherein the plating current density is 0.5 to 1.5 A/dm^2.

18(original). The process of claim 14 wherein the periphery of the blind via hole has a diameter of from about 20 to 50 μm, and wherein the plating current density is 0.5 to 1 A/dm^2.

A1

19(original). A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer formed on the first surface, onto a base material on which a predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to said base material;

removing a predetermined amount of said metal layer to form an opening having a first diameter at a position where a connection with said wiring pattern is to be attained;

irradiating a laser beam toward said resin layer through said resin removed region to form a blind via hole having a diameter smaller than that of said opening, so that said wiring pattern is exposed at a bottom of said blind via hole and a step portion of the resin substrate remains adjacent a periphery of said blind via hole;

electroless plating to form an electroless plated film on said exposed wiring pattern, a side wall of said blind via hole, the step portion of said exposed resin layer, and at least a portion of the metal layer adjacent a periphery of said opening;

electro plating at a density of electric current of less than about 1 A/dm^2 to form an electro plated film on said electroless plated film; and

after said electro plating, etching said metal layer to form a predetermined wiring pattern.

A 1

20(original). The process of claim 19 wherein the periphery of the blind via hole has a diameter of from about 20 to 50 μm, and wherein the plating current density is 0.5 to 1 A/dm^2.